IN THE CLAIMS:

1. (currently amended) A communication system, comprising:

a. a memory structure receiving and storing undecoded symbols, each of the undccoded symbols having a unique pointer associated therewith and one of the undecoded symbols being a most likely symbol; and

b. a pointer selector processing the unique pointers according to a predetermined selection operation ~~and selecting operation~~ and selecting a most likely pointer uniquely associated with the most likely symbol, the decoder outputting the most likely symbol thereby.

2. (cancelled)

3. (original) The communication system of claim 1, wherein the undecoded symbols are representative of potential received signals.

4.-10. (cancelled)

11. (currently amended) A decoder, comprising:

a. a memory structure receiving ~~a~~and storing undecoded symbols, each of the undecoded symbols having a unique pointer associated therewith and one of the undecoded symbols being a most likely symbol; and

b. a pointer selector processing the unique pointers according to a predetermined selection operation and selecting a most likely pointer uniquely associated with the most likely symbol, the decoder outputting the most likely symbol thereby.

12. (cancelled)

13. (original) The decoder of claim 11, wherein the undecoded symbols are representative of potential received signals.

14.-35. (cancelled)

36. (original) A method for processing symbolic communication signals, comprising:

a. receiving potential symbols including a most likely symbol;

b. associating each of the received potential symbols with a unique pointer;

c. processing the unique pointers associated with selected ones of the received potential symbols to determine a most likely pointer using a predetermined selection operation; and

d. selecting the most likely symbol using the most likely pointer.

37. (original) The method of claim 36, further comprising storing the potential symbols in a memory structure.

38. (original) The method of claim 37, wherein the memory structure is capable of performing a read operation and a write operation in one clock cycle.

39.-42. (cancelled)